MOSFETs Silicon N-Channel MOS (DTMOSⅢ)

TK45J60V

1. Applications

- Switching Voltage Regulators

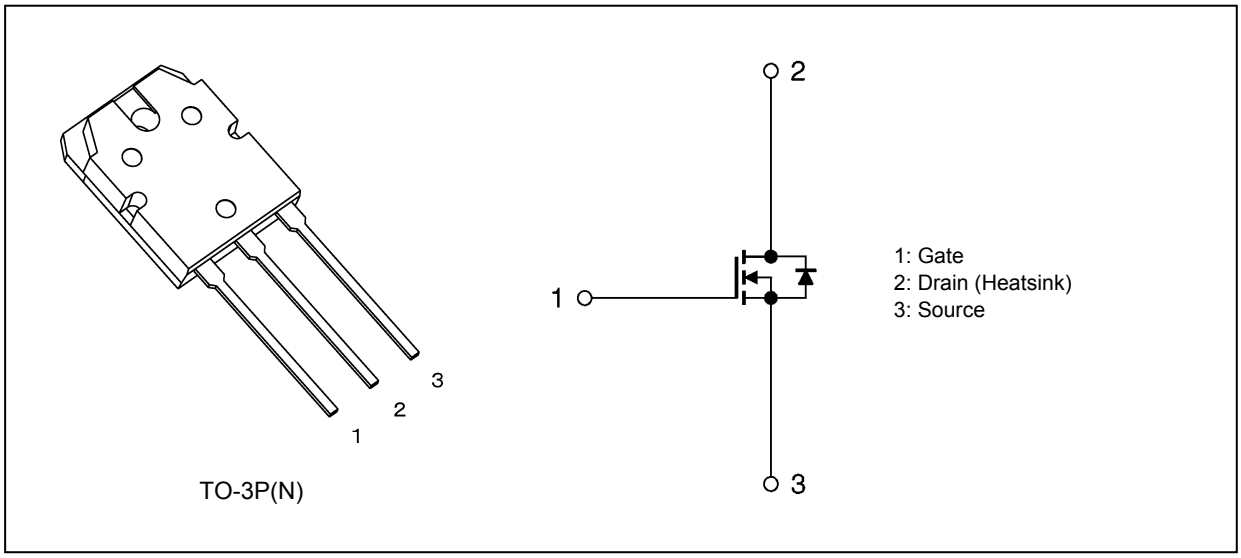
2. Features

(1) Low drain-source on-resistance: $R_{DS(ON)}$ = 0.055 Ω (typ.)
by used to Super Junction Structure : DTMOS

(2) Easy to control Gate switching

(3) Enhancement mode: V_{th} = 2.5 to 3.5 V (V_{DS} = 10 V, I_D = 2.25 mA)

3. Packaging and Internal Circuit



4. Absolute Maximum Ratings (Note) (Ta = 25°C unless otherwise specified)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	600	V
Gate-source voltage		V_{GSS}	±30	
Drain current (DC)	(Note 1)	I_D	45	A
Drain current (pulsed)	(Note 1)	I_{DP}	90	
Power dissipation	(T_c = 25°C)	P_D	370	W
Single-pulse avalanche energy	(Note 2)	E_{AS}	578	mJ
Avalanche current		I_{AR}	22.5	A
Reverse drain current (DC)	(Note 1)	I_{DR}	45	
Reverse drain current (pulsed)	(Note 1)	I_{DRP}	90	
Channel temperature		T_{ch}	150	°C
Storage temperature		T_{stg}	-55 to 150	
Mounting torque		TOR	0.8	N · m

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	$R_{th(ch-c)}$	0.338	°C/W
Channel-to-ambient thermal resistance	$R_{th(ch-a)}$	50	

Note 1: Ensure that the channel temperature does not exceed 150°C.
Note 2: V_{DD} = 90 V, T_{ch} = 25°C (initial), L = 2.0 mH, R_G = 25 Ω, I_{AR} = 22.5 A

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

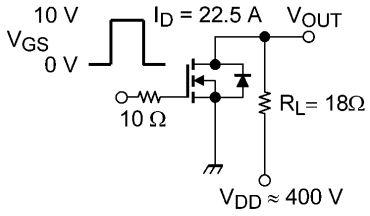
6. Electrical Characteristics

6.1. Static Characteristics (Ta = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V	—	—	±1	μA
Drain cut-off current	I_{DSS}	V_{DS} = 600 V, V_{GS} = 0 V	—	—	1	
Drain-source breakdown voltage	$V_{(BR)DSS}$	I_D = 10 mA, V_{GS} = 0 V	600	—	—	V
Gate threshold voltage	V_{th}	V_{DS} = 10 V, I_D = 2.25 mA	2.5	—	3.5	
Drain-source on-resistance	$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 22.5 A	—	0.055	0.065	Ω

6.2. Dynamic Characteristics (Ta = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	V_{DS} = 300 V, V_{GS} = 0 V, f = 0.1 MHz	—	4800	—	pF
Reverse transfer capacitance	C_{rss}		—	8	—	
Output capacitance	C_{oss}		—	120	—	
Effective output capacitance	$C_{o(er)}$	V_{DS} = 0 to 400 V, V_{GS} = 0 V	—	190	—	
Gate resistance	r_g	V_{DS} = OPEN, f = 1 MHz	—	1.8	—	Ω
Switching time (rise time)	t_r	See Figure 6.2.1	—	60	—	ns
Switching time (turn-on time)	t_{on}		—	95	—	
Switching time (fall time)	t_f		—	35	—	
Switching time (turn-off time)	t_{off}		—	190	—	



Duty ≤ 1%, t_w = 10 μs

Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics (Ta = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	V_{DD} ≈ 400 V, V_{GS} = 10 V, I_D = 45 A	—	110	—	nC
Gate-source charge 1	Q_{gs1}		—	28	—	
Gate-drain charge	Q_{gd}		—	46	—	
MOSFET dv/dt ruggedness	dv/dt	V_{DD} = 0 to 400 V, I_D = 22.5 A	50	—	—	V/ns

6.4. Source-Drain Characteristics (Ta = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Diode forward voltage	V_{DSF}	I_{DR} = 45 A, V_{GS} = 0 V	—	—	-1.7	V
Reverse recovery time	t_{rr}	I_{DR} = 45 A, V_{GS} = 0 V $-dI_{DR}/dt$ = 200 A/μs	—	520	—	ns
Reverse recovery charge	Q_{rr}		—	20	—	μC
Peak reverse recovery current	I_{rr}		—	70	—	A
Diode dv/dt ruggedness	dv/dt	I_{DR} = 45 A, V_{GS} = 0 V, V_{DD} = 400 V	15	—	—	V/ns

7. Marking (Note)

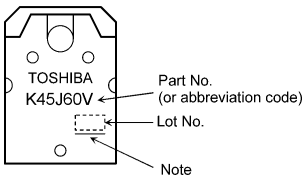


Fig. 7.1 Marking

Note: A line under a Lot No. identifies the indication of product Labels.
Not underlined: [[Pb]]/INCLUDES > MCV
Underlined: [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]
Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product.
The RoHS is the Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

8. Characteristics Curves (Note)

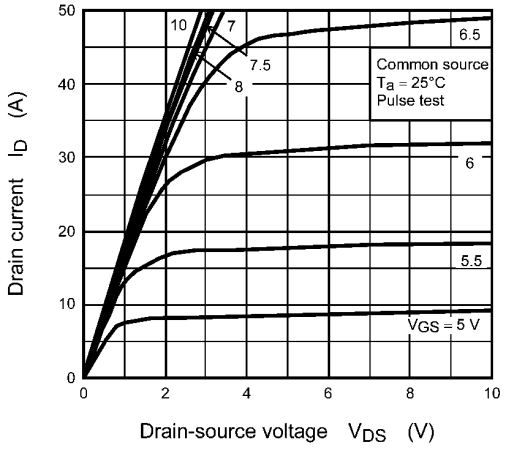


Fig. 8.1 I_D - V_{DS}

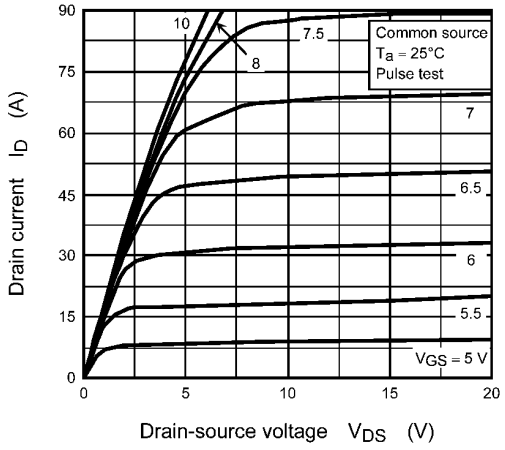


Fig. 8.2 I_D - V_{DS}

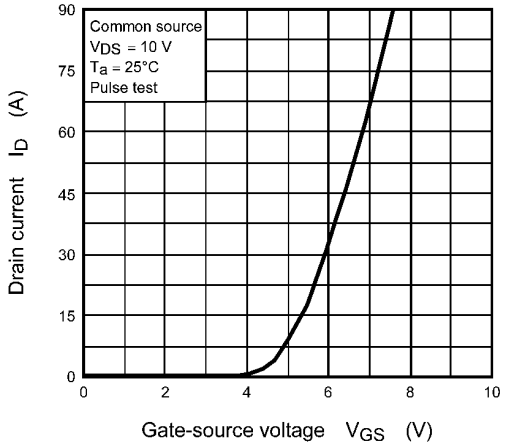


Fig. 8.3 I_D - V_{GS}

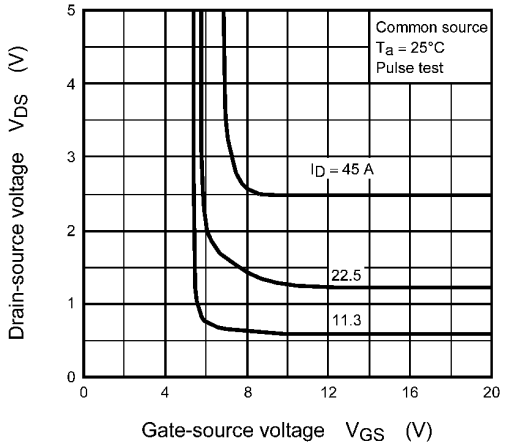


Fig. 8.4 V_{DS} - V_{GS}

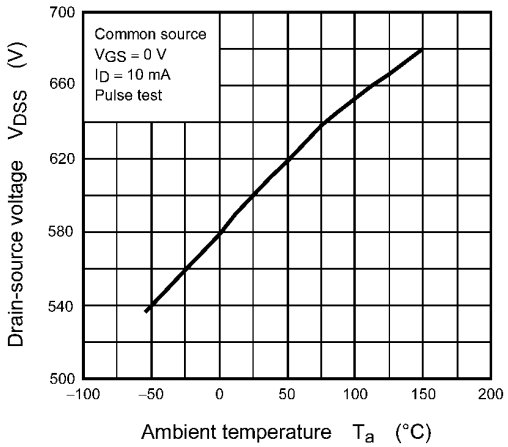


Fig. 8.5 V_{DSS} - T_a

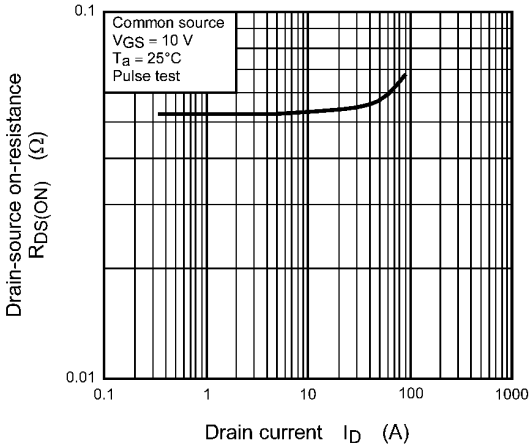


Fig. 8.6 $R_{DS(ON)}$ - I_D

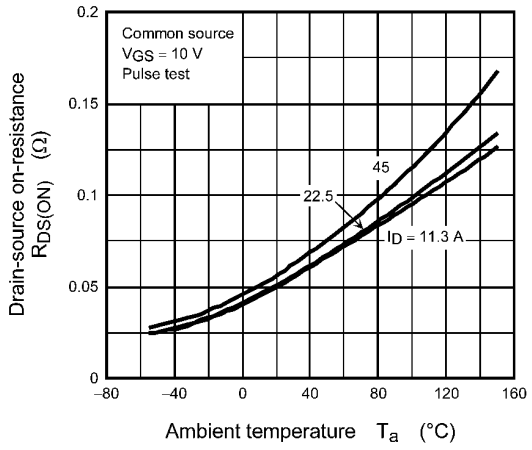


Fig. 8.7 $R_{DS(ON)}$ - T_a

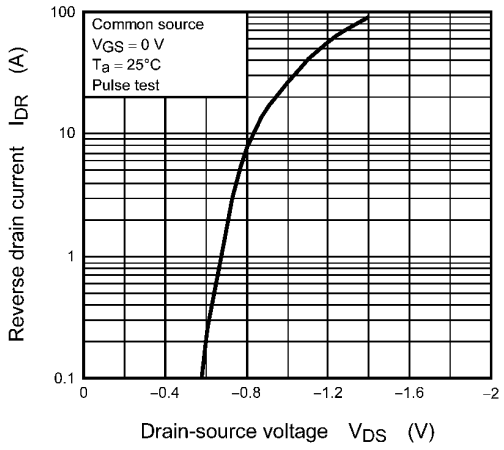


Fig. 8.8 I_{DR} - V_{DS}

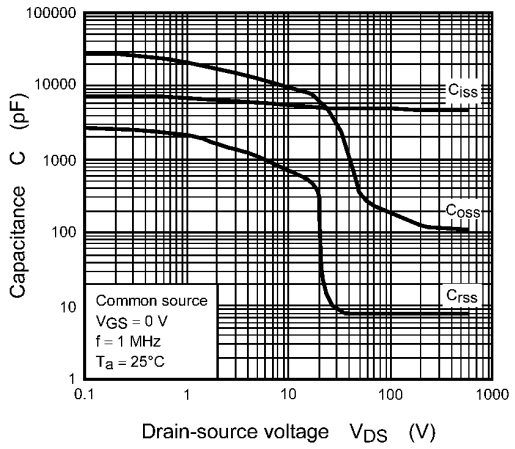


Fig. 8.9 C - V_{DS}

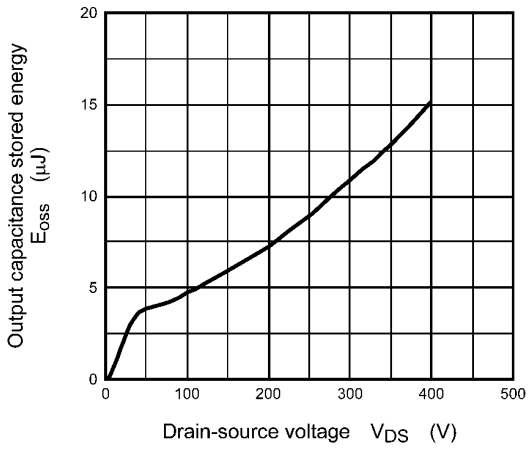


Fig. 8.10 E_{OSS} - V_{DS}

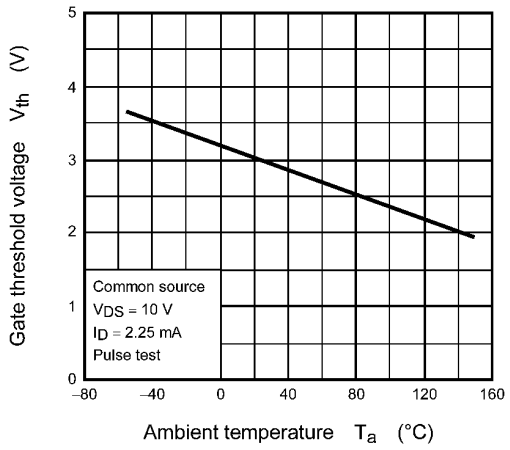


Fig. 8.11 V_{th} - T_a

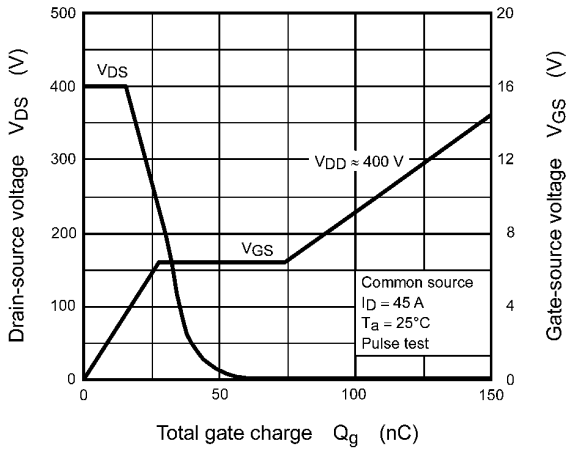


Fig. 8.12 Dynamic Input/Output Characteristics

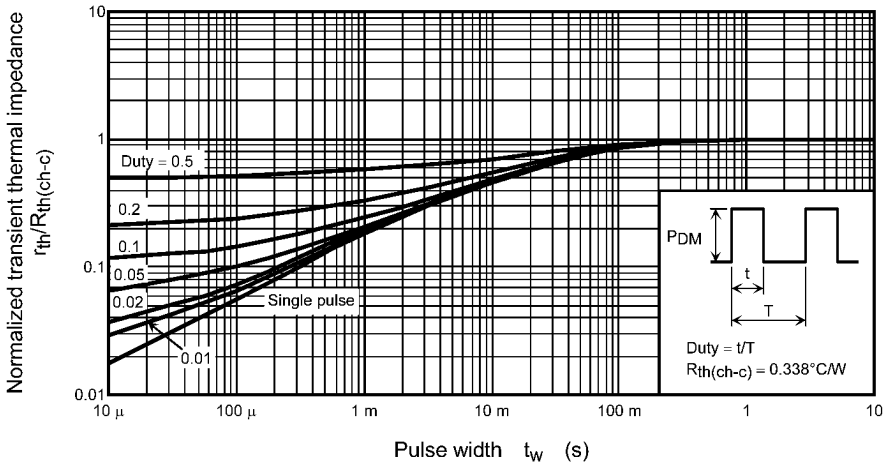


Fig. 8.13 r_{th} - t_w
(Guaranteed Maximum)

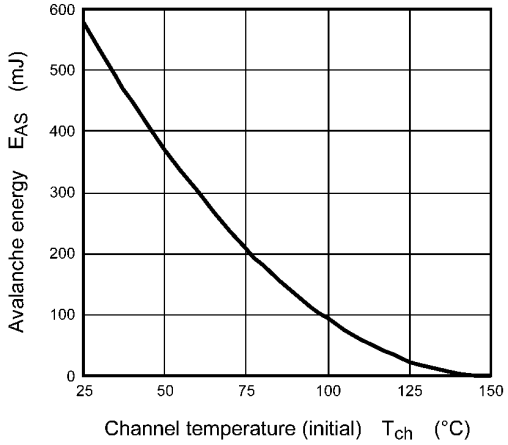


Fig. 8.14 E_{AS} - T_{ch}
(Guaranteed Maximum)

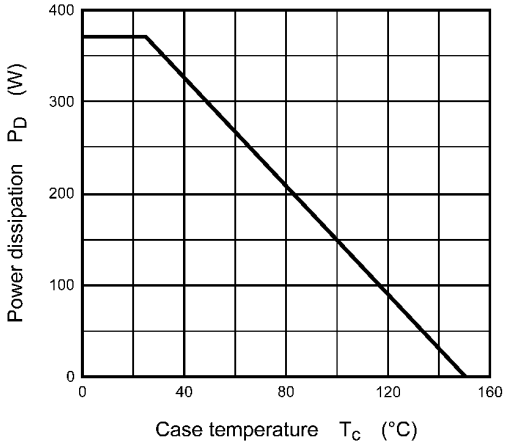
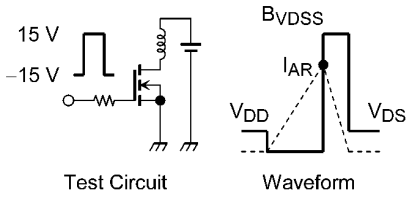


Fig. 8.15 P_D - T_c
(Guaranteed Maximum)



$R_G = 25\ \Omega$, $V_{DD} = 90$ V $E_{AS} = \frac{1}{2} \cdot L \cdot I_{AR}^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$

Fig. 8.16 Test Circuit/Waveform

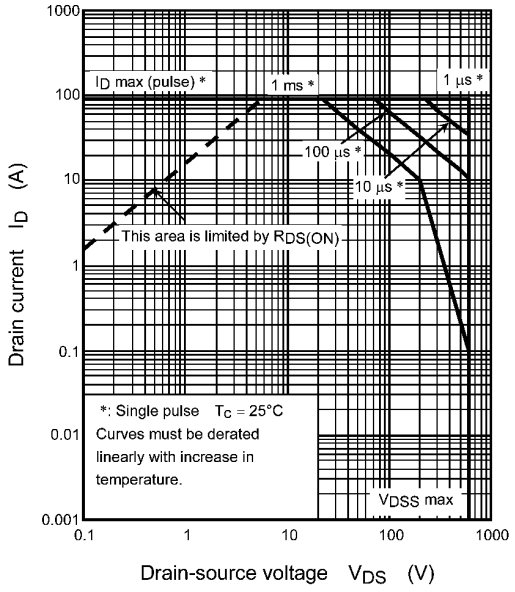
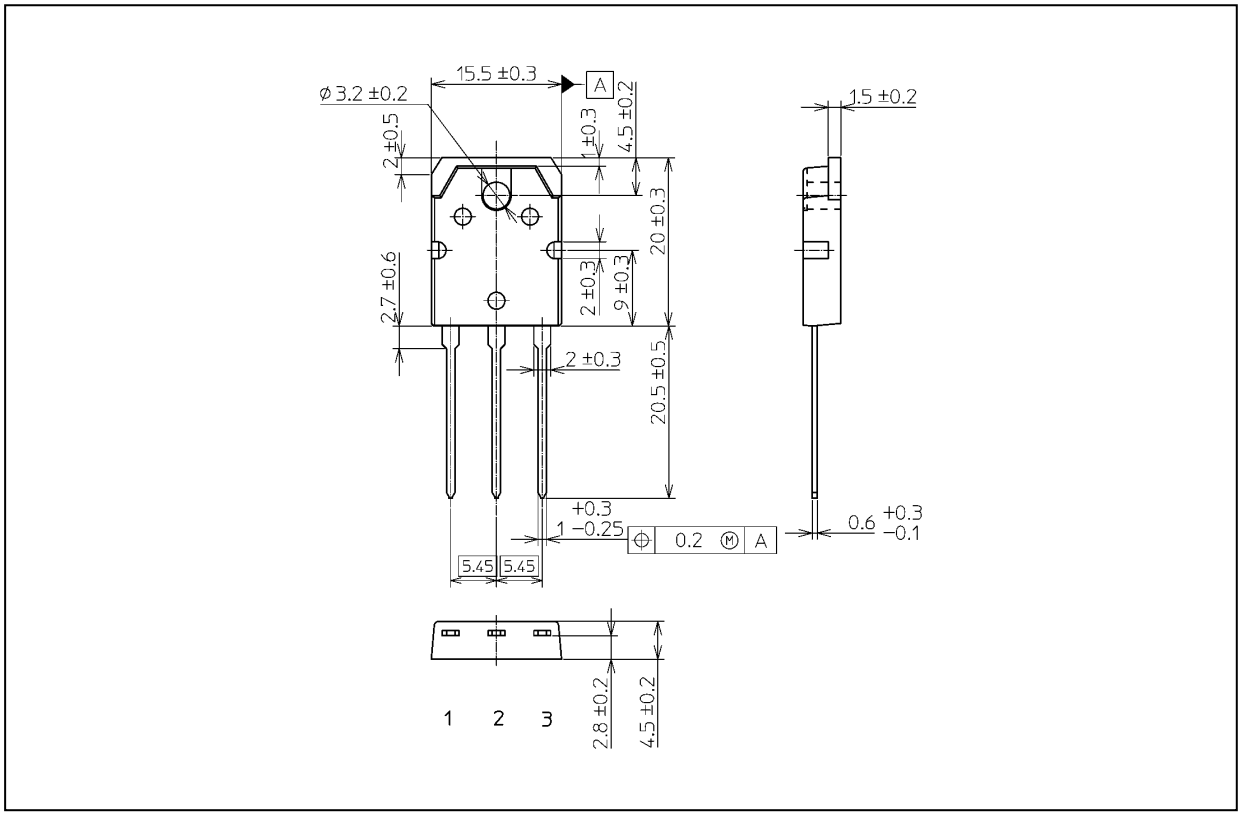


Fig. 8.17 Safe Operating Area (Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test.

Package Dimensions

Unit: mm



Weight: 4.6 g (typ.)

Package Name(s)
JEITA: SC-65
TOSHIBA: 2-16C1S
Nickname: TO-3P(N)

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